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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/678,479 | 10/03/2003 | Vladimir Tsukanov | 011775-013410US | 1443 |

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| EXAMINER | |
|---|---|
| VU, DAVID | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/678,479 | TSUKANOV ET AL. |
| | Examiner | Art Unit |
| | DAVID VU | 2818 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *25-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☒ Claim(s) *23 and 24* is/are objected to.

8)☒ Claim(s) *1-27* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/07/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

# DETAILED ACTION

## Election/Restrictions

1. Applicant's election without traverse of Group I (Claims 1-24) on 08/03/2004 is acknowledged.

Claims 25-27 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 08/03/04.

## Drawings

2. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

## *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 19 recites the limitation "the first doped region" in page 18, lines 6. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 22 recites the limitation "the first doped region" in page 18, lines 7. There is insufficient antecedent basis for this limitation in the claim.

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2 and 8-18 are rejected under 35 U. S. C. 102(b) as being anticipated by Hshieh et al. (US Pat. 5,689,128, herein after Hshieh '128).

Regarding claim 1, Hshieh '128 discloses a power semiconductor device, comprising: a substrate having an upper surface and a lower surface, the substrate having a trench; first and second doped regions 16 provided proximate the upper surface of the substrate; a first source region 20 provided within the first doped region 16; a second source region 20 provided within the second doped region 16; and a gate 22 provided between the first and second source regions (fig. 1), the gate including a first portion extending downward into the trench, wherein a depth of the trench is no more than a depth of the first doped region (col. 3, lines 16-19 and lines 25-27).

Regarding claim 2, Hshieh '128 discloses a drain region 10 provided proximate the lower surface of the substrate (col. 3, lines 4-6).

Regarding claim 8, Hshieh '128 discloses the depth of the first doped region 16 is no more than about 5 micron (col. 3, lines 16-19).

Regarding claim 9, Hshieh '128 discloses the depth of the trench is no more than about 2.5 micron (col. 3, lines 25-26).

Regarding claim 10, Hshieh '128 discloses the first portion of the gate includes a planar portion (channel region) that is substantially parallel to the upper surface of the substrate (fig. 1 and col. 3, lines 59-62).

Regarding claims 11-14, Hshieh '128 discloses the planar portion is longer than about 1-4 micron (fig. 1 and col. 3, lines 59-62).

Regarding claim 15, Hshieh '128 discloses the device is a power MOSFET (col.1, lines 47-49).

Regarding claim 16, Hshieh '128 discloses a power semiconductor device, comprising: a substrate having an upper surface and a lower surface, the substrate having a trench; a first doped region 16 provided proximate the upper surface of the substrate; a first source region 20 provided within the first doped region 16; and a gate 22 provided adjacent the first source region 20 (fig. 1), the gate including a first portion provided within the trench, wherein a depth of the trench is no more than a depth of the first doped region (col. 3, lines 16-19 and lines 25-27).

Regarding claim 17, Hshieh '128 discloses a drain region 10 provided proximate the lower surface of the substrate (col. 3, lines 4-6).

Regarding claim 18, Hshieh '128 discloses the first portion of the gate is substantially parallel to the upper surface of the substrate and is longer than 2 micron (fig. 1 and col. 3, lines 59-62).

6. Claims 19 and 22 are rejected under 35 U. S. C. 102(b) as being anticipated by Hshieh et al. (US Pat. 5,629,543, herein after Hshieh '543).

Regarding claim 19, Hshieh '543 discloses a power semiconductor device, comprising: a substrate having a first surface and a second surface, the substrate having a trench having a first depth (fig. 3C); a doped region 18 provided proximate the first surface of the substrate and having a second depth; a source region 20 provided within the first doped region 18 and proximate the first surface; and a gate 30A/30B provided adjacent the source region 20, the gate including a first portion provided within the trench and a second portion provide outside of the trench (col. 3, lines 25-29); and the first portion having a length (col. 4, line 49) that is greater than the first depth of the trench (col. 4, lines 21-22); {See also **Takeuchi et al.** (US Pat. 6,133,587) (col. 8; lines 47-54 and fig. 14) for evidence of the state of the art in which the hexagonal cell structure comprises a gate including a first portion provided within the shallow trench and a second portion provide outside of the trench}.

Regarding claim 22, Hshieh '543 discloses a method for fabricating a power semiconductor device, comprising: forming a shallow trench on a substrate having a first surface and a second surface, the shallow trench having a first depth and a width (fig. 3C), the width of the shallow trench (col. 4, line 49) being greater than the first depth of the shallow trench (col. 4, lines 21-22); forming a doped region 18 provided proximate the first surface of the substrate and having a second depth; forming a source region 20 provided within the first doped region 18 and proximate the first surface; and forming a gate structure 30A/30B provided adjacent the source region 20, the gate structure including a first portion provided within the shallow trench and a second portion provide outside of the trench (col. 3, lines 25-29); {See also **Takeuchi et al.** (US

Pat. 6,133,587) (col. 8; lines 47-54 and fig. 14) for evidence of the state of the art in which the hexagonal cell structure comprises a gate including a first portion provided within the shallow trench and a second portion provide outside of the trench}.

## *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 3 and 4 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Hshieh et al. (US Pat. 5,689,128, herein after Hshieh '128) in view of Takeuchi et al. (US Pat. 6,133,587, herein after Takeuchi)

Regarding claim 3, Hshieh '128 teaches a power semiconductor device as describe above but fails to disclose the gate further comprises a second portion provided overlying the substrate and extending toward the first source region. However, Takeuchi teaches the gate structure including a first portion provided within the shallow trench and a second portion provide outside of the trench (col. 8; lines 47-54 and fig. 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted gate structure such as taught by Takeuchi in place of the gate structure of Hshieh device, because it would have been a mere substitution of well known art recognized equivalent gate structure for provide electrical contact.

Regarding claim 4, Hshieh '128 discloses the trench has smooth, continuous sidewalls formed using a deep oxidation process (col. 4, lines 63-66).

8. Claims 5-7 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Hshieh et al. (US Pat. 5,689,128, herein after Hshieh '128) in view of Hshieh et al. (US Pat. 5,629,543, herein after Hshieh '543).

Hshieh '128 teaches a power semiconductor device as describe above but fails to disclose a length of the first portion of the gate is greater than the depth of the trench. However, Hshieh '543 teaches a length of the first portion of the gate (col. 4, line 49) that is greater than the depth of the trench (col. 4, lines 21-22) and a ratio of a length of the first portion of the gate to the depth of the trench is about 2:1.7. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hshieh '128 by incorporating a power semiconductor device as taught by Hshieh '543 since the specification cotains no disclosure of either the critical nature of the claimed device (i.e. - a ratio of a length of the first portion of the gate to the depth

of the trench is at least 1.5:1; 2.5:1) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the Applicant must show that the chosen limitation are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

9. Claims 20 and 21 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Hshieh et al. (US Pat. 5,629,543, herein after Hshieh '543) in view of Hshieh et al. (US Pat. 5,689,128, herein after Hshieh '128).

Regarding claim 20, Hshieh '543 teaches a power semiconductor device as describe above but fails to disclose the depth of the trench is no more than the depth of the doped region. However, Hshieh '128 teaches depth of the trench is no more than a depth of the doped region (col. 3, lines 16-19 and lines 25-27) and the device further comprising: a drain region 10 provided proximate the second surface of the substrate (col. 3, lines 4-6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hshieh '543 by incorporating a power semiconductor device as taught by Hshieh '128 to reduce diffusion time to establish the depth of the doped region (col. 3, lines 50-58).

Regarding claim 21, Hshieh '128 teaches the first portion is substantially planar and is longer than 2 micron (fig. 1 and col. 3, lines 59-62).

## *Allowable Subject Matter*

10. Claims 23 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record, either singularly or in combination, does not disclose or suggest an Applicant's claimed method for fabricating a power semiconductor device, particularly characterized by: "forming the shallow trench includes: etching the substrate to form an intermediate trench having a third depth that is less than the first depth; forming a first oxide layer within the intermediate layer; and removing the oxide layer formed within the intermediate trench, wherein a resulting trench from the removal of the oxide layer has a fourth depth that is greater than the third depth."

## Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Vu

September 15, 2004.